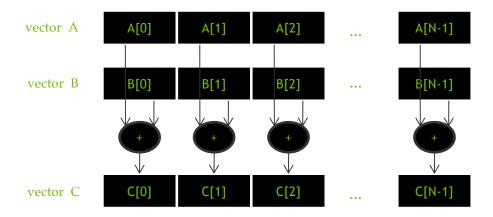


## Objective

- To learn about CUDA threads, the main mechanism for exploiting of data parallelism
  - Hierarchical thread organization
  - Launching parallel execution
  - Thread index to data index mapping



### Data Parallelism - Vector Addition Example

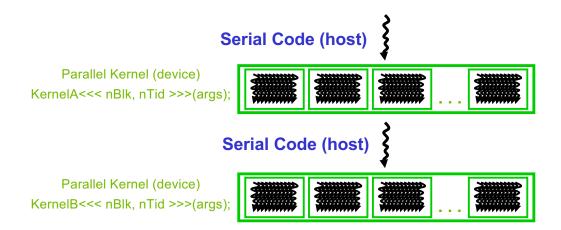


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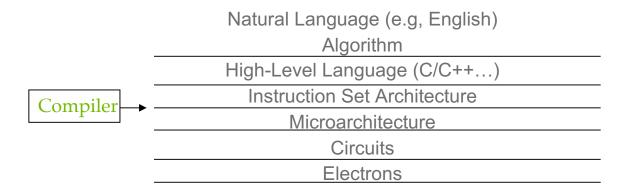


#### **CUDA Execution Model**

- Heterogeneous host (CPU) + device (GPU) application C program
  - Serial parts in host C code
  - Parallel parts in device SPMD kernel code



### From Natural Language to Electrons



©Yale Patt and Sanjay Patel, From bits and bytes to gates and beyond

NIDIA 🕑

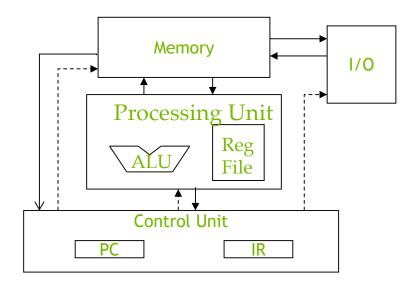
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## A program at the ISA level

- A program is a set of instructions stored in memory that can be read, interpreted, and executed by the hardware.
  - Both CPUs and GPUs are designed based on (different) instruction sets
- Program instructions operate on data stored in memory and/or registers.

#### A Thread as a Von-Neumann Processor

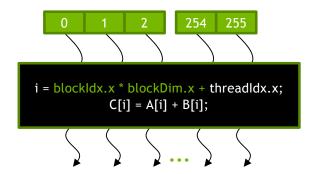
A thread is a "virtualized" or "abstracted" **Von-Neumann Processor** 





### **Arrays of Parallel Threads**

- A CUDA kernel is executed by a grid (array) of threads
  - All threads in a grid run the same kernel code (Single Program Multiple Data)
  - Each thread has indexes that it uses to compute memory addresses and make control decisions



### Thread Blocks: Scalable Cooperation

#### Thread Block 0 Thread Block 1 Thread Block N-1 i = blockIdx.x \* blockDim.x + i = blockIdx.x \* blockDim.x + i = blockIdx.x \* blockDim.x + threadIdx.x; threadIdx.x; threadIdx.x; C[i] = A[i] + B[i];C[i] = A[i] + B[i];C[i] = A[i] + B[i];

- Divide thread array into multiple blocks
  - Threads within a block cooperate via shared memory, atomic operations and barrier synchronization
  - Threads in different blocks do not interact



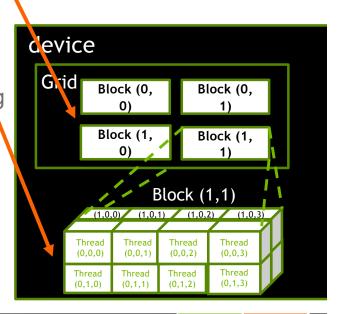


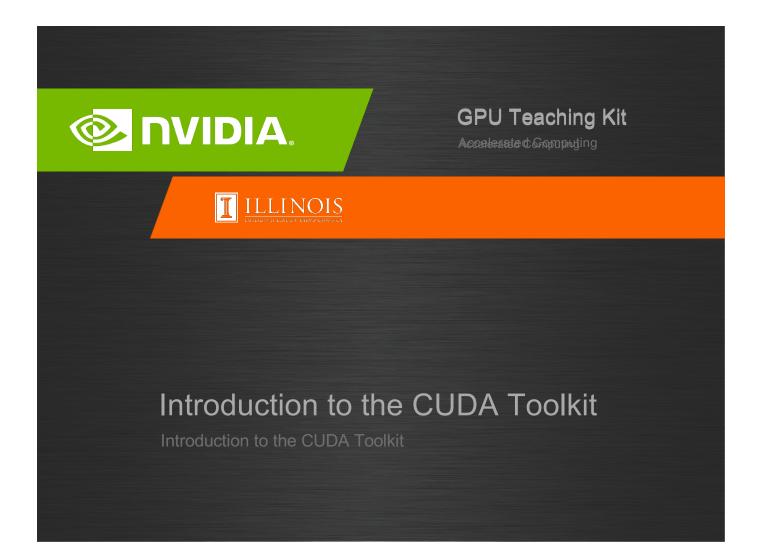
#### blockldx and threadldx

- Each thread uses indices to decide what data to work on
  - blockldx: 1D, 2D, or 3D (CUDA 4.0)

threadIdx: 1D, 2D, or 3D

- Simplifies memory addressing when processing multidimensional data
  - Image processing
  - Solving PDEs on volumes

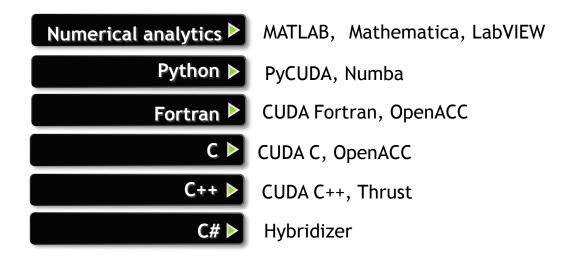




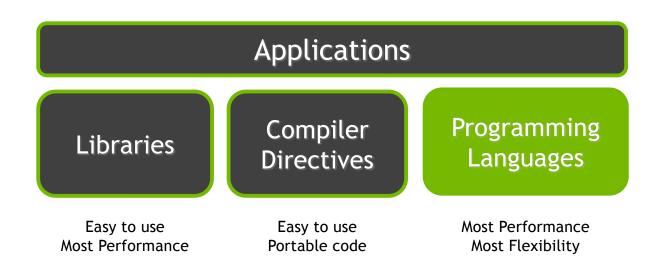
## Objective

- To become familiar with some valuable tools and resources from the CUDA Toolkit
  - Compiler flags
  - Debuggers
  - Profilers

### **GPU Programming Languages**



#### CUDA - C



## **NVCC Compiler**

- NVIDIA provides a CUDA-C compiler
  - nvcc
- NVCC compiles device code then forwards code on to the host compiler (e.g. g++)
- Can be used to compile & link host only applications

## Example 1: Hello World

```
#include <cstdio>
int main() {
   printf("Hello World!\n");
   return 0;
```

#### Instructions:

- 1. Build and run the hello world code
- 2. Modify Makefile to use nvcc instead of g++
- 3. Rebuild and run

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## **CUDA Example 1: Hello World**

```
#include <cstdio>
__global__ void mykernel(void) {
int main(void) {
   mykernel <<<1,1>>>();
   printf("Hello World!\n");
```

#### Instructions:

- 1. Add kernel and kernel launch to main.cc
- 2. Try to build





## **CUDA Example 1: Build Considerations**

- Build failed
  - nvcc only parses .cu files for CUDA
- Fixes:
  - Rename main.cc to main.cu
  - OR
  - nvcc -x cu
    - Treat all input files as .cu files

#### Instructions:

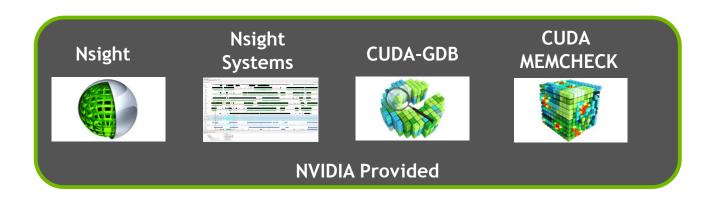
- 1. Rename main.cc to main.cu
- 2. Rebuild and Run

#### Hello World! with Device Code

```
#include <cstdio>
__global__ void mykernel(void) {
int main(void) {
   mykernel<<<1,1>>>();
   printf("Hello World!\n");
   return 0;
Output:
$ nvcc main.cu
$ ./a.out
Hello World!
```

– mykernel (does nothing, somewhat anticlimactic!)

## **Developer Tools - Debuggers**





https://developer.nvidia.com/debugging-solutions

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### Compiler Flags

- Remember there are two compilers being used
  - NVCC: Device code
  - Host Compiler: C/C++ code
- NVCC supports some host compiler flags
  - If flag is unsupported, use –Xcompiler to forward to host
    - e.g. –Xcompiler –fopenmp
- Debugging Flags
  - -g: Include host debugging symbols
  - -G: Include device debugging symbols
  - -lineinfo: Include line information with symbols



#### **CUDA-MEMCHECK**

- Memory debugging tool
  - No recompilation necessary
    - %> cuda-memcheck ./exe
- Can detect the following errors
  - Memory leaks
  - Memory errors (OOB, misaligned access, illegal instruction, etc)
  - Race conditions
  - Illegal Barriers
  - Uninitialized Memory
- For line numbers use the following compiler flags:
  - -Xcompiler -rdynamic -lineinfo

http://docs.nvidia.com/cuda/cuda-memcheck



### Example 2: CUDA-MEMCHECK

#### Instructions:

- Build & Run Example 2
   Output should be the numbers 0-9
   Do you get the correct results?
- 2. Run with cuda-memcheck %> cuda-memcheck ./a.out
- 3. Add nvcc flags "-Xcompiler -rdynamic lineinfo"
- 4. Rebuild & Run with cuda-memcheck
- 5. Fix the illegal write

http://docs.nvidia.com/cuda/cuda-memcheck

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#### **CUDA-GDB**

- cuda-gdb is an extension of GDB
  - Provides seamless debugging of CUDA and CPU code
- Works on Linux and Macintosh
  - For a Windows debugger use NVIDIA Nsight Eclipse Edition or Visual Studio Edition

http://docs.nvidia.com/cuda/cuda-gdb



### Example 3: cuda-gdb

# **Instructions:** 1. Run exercise 3 in cuda-gdb %> cuda-gdb --args ./a.out 2. Run a few cuda-gdb commands: (cuda-gdb) b main (cuda-gdb) c (cuda-gdb) cuda thread (cuda-gdb) cuda thread 10 (cuda-gdb) cuda thread 10 (cuda-gdb) cuda block (cuda-gdb) cuda block (cuda-gdb) cuda block //print current block (cuda-gdb) cuda block 1 (cuda-gdb) cuda block //print current thread 10 (cuda-gdb) cuda thread 10 (cuda-gdb) cuda thread 10 (cuda-gdb) cuda thread 10 (cuda-gdb) cuda block //print current thread 10 (cuda-gdb) cuda block //print current bloc (cuda-gdb) cuda block 1 (cuda-gdb) d 3. Fix Bug

http://docs.nvidia.com/cuda/cuda-gdb

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## **Developer Tools - Profilers**



https://developer.nvidia.com/performance-analysis-tools

<sup>3rd</sup> Partv

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#### **NVPROF**

#### Command Line Profiler

- Compute time in each kernel
- Compute memory transfer time
- Collect metrics and events
- Support complex process hierarchy's
- Collect profiles for NVIDIA Visual Profiler
- No need to recompile





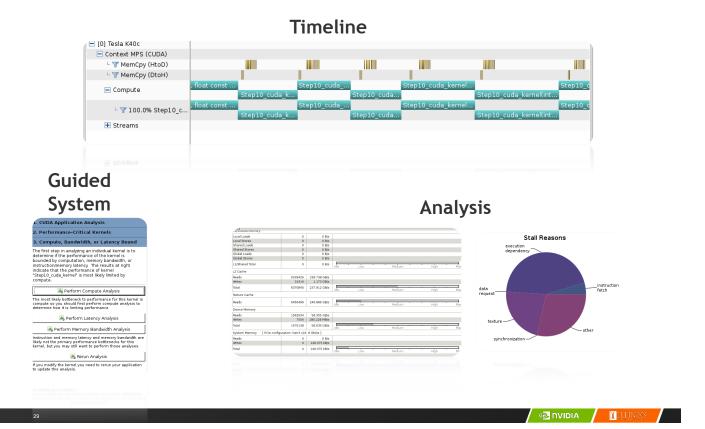
### Example 4: nvprof

#### Instructions:

- Collect profile information for the matrix add example %> nvprof ./a.out
- 2. How much faster is add\_v2 than add\_v1?
- 3. View available metrics
  - %> nvprof --query-metrics
- 4. View global load/store efficiency
  - %> nvprof --metrics gld\_efficiency,gst\_efficiency ./a.out
- 5. Store a timeline to load in NVVP
  - %> nvprof -o profile.timeline ./a.out
- 6. Store analysis metrics to load in NVVP
  - %> nvprof -o profile.metrics --analysis-metrics ./a.out



## NVIDIA's Visual Profiler (NVVP)



### **Example 4: NVVP**

#### Instructions:

1. Import nvprof profile into NVVP

Launch nvvp

Click File/ Import/ Nvprof/ Next/ Single process/ Next / Browse Select profile.timeline

Add Metrics to timeline

Click on 2<sup>nd</sup> Browse

Select profile.metrics

Click Finish

2. Explore Timeline

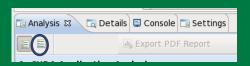
Control + mouse drag in timeline to zoom in

Control + mouse drag in measure bar (on top) to measure time

### **Example 4: NVVP**

#### Instructions:

- 1. Click on a kernel
- 2. On Analysis tab click on the unguided analysis



2. Click Analyze All Explore metrics and properties What differences do you see between the two kernels?

#### Note:

If kernel order is non-deterministic you can only load the timeline or the metrics but not both.

If you load just metrics the timeline looks odd but metrics are correct.

on and the state of the state

### **Example 4: NVVP**

Let's now generate the same data within NVVP

Click File / New Session / Browse
 Select Example 4/a.out
 Click Next / Finish
 Click on a kernel
 Select Unguided Analysis
 Click Analyze All

#### **NVTX**

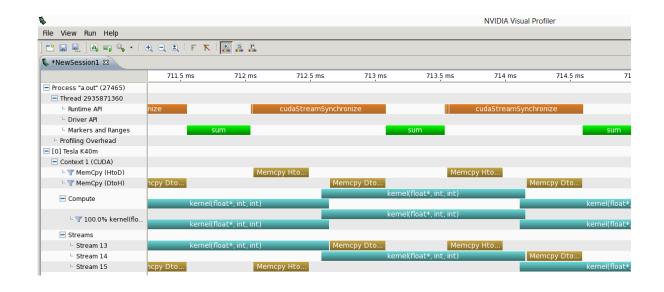
- Our current tools only profile API calls on the host
  - What if we want to understand better what the host is doing?
- The NVTX library allows us to annotate profiles with ranges
  - Add: #include <nvToolsExt.h>
  - Link with: -InvToolsExt
- Mark the start of a range
  - nvtxRangePushA("description");
- Mark the end of a range
  - nvtxRangePop();
- Ranges are allowed to overlap

http://devblogs.nvidia.com/parallelforall/cuda-pro-tip-generate-custom-application-profile-timelines-nvtx/





#### **NVTX** Profile





#### **NSIGHT**

- CUDA enabled Integrated Development Environment
  - Source code editor: syntax highlighting, code refactoring, etc
  - Build Manger
  - Visual Debugger
  - Visual Profiler
- Linux/Macintosh
  - Editor = Eclipse
  - Debugger = cuda-gdb with a visual wrapper
  - Profiler = NVVP
- Windows
  - Integrates directly into Visual Studio
  - Profiler is NSIGHT VSE



### **Example 4: NSIGHT**

Let's import an existing Makefile project into NSIGHT

#### Instructions:

- 1. Run nsight Select default workspace
- 2. Click File / New / Makefile Project With Existing CodeTest
- 3. Enter Project Name and select the Example 15 directory
- 4. Click Finish
- 5. Right Click On Project / Properties / Run Settings / New / C++ **Application**
- 6. Browse for Example 4/a.out
- 7. In Project Explorer double click on main.cu and explore source
- 8. Click on the build icon
- 9. Click on the run icon
- 10. Click on the profile icon

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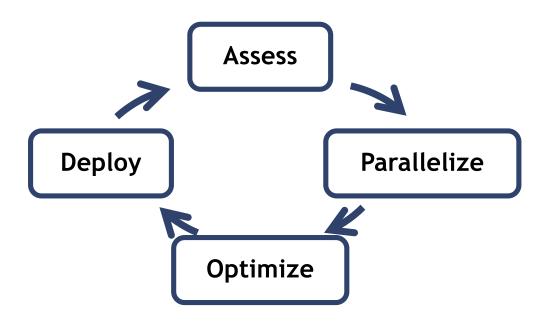
## **Profiler Summary**

- Many profile tools are available
- NVIDIA Provided
  - NVPROF: Command Line
  - NVVP: Visual profiler
  - NSIGHT: IDE (Visual Studio and Eclipse)
- 3<sup>rd</sup> Party
  - TAU
  - VAMPIR

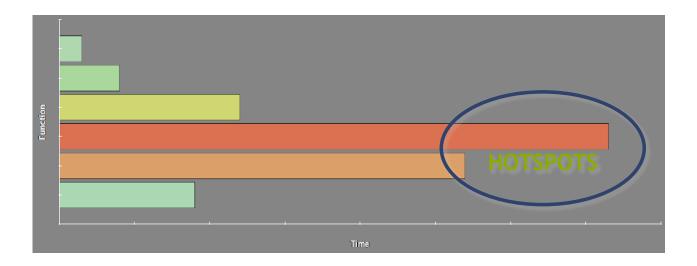
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## Optimization



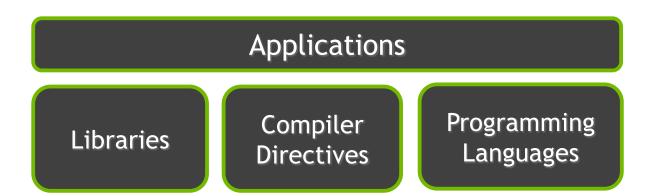
#### **Assess**



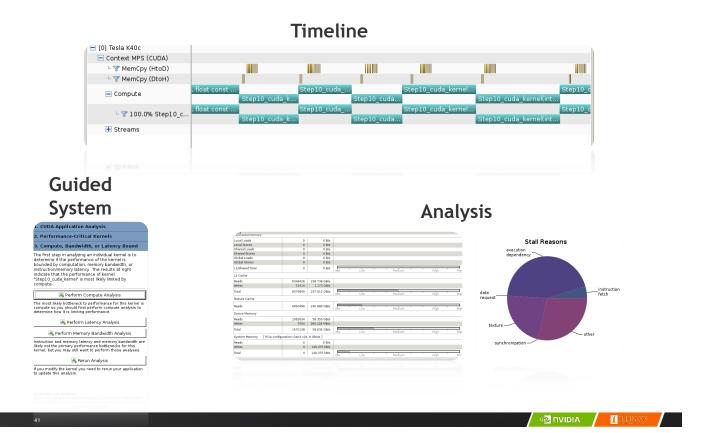
- Profile the code, find the hotspot(s)
- Focus your attention where it will give the most benefit

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### **Parallelize**



## **Optimize**



## **Bottleneck Analysis**

- Don't assume an optimization was wrong
- Verify if it was wrong with the profiler

129 GB/s **>** 84 GB/s

L1/Shared Memory						
Local Loads	0	0 B/s				
Local Stores	0	0 B/s				
Shared Loads	2097152	1,351.979 GB/s				
Shared Stores	131072	84.499 GB/s				
Global Loads	131072	42.249 GB/s				
Global Stores	131072	42.249 GB/s				
Atomic	0	0 B/s				
L1/Shared Total	2490368	1,520.977 GB/s	Idle	Low	Medium	

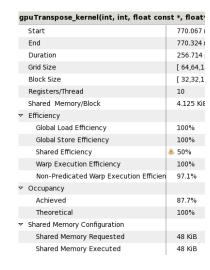
g	puTranspose_kernel(int, int, float con	St	*, float*)
	Start		547.303 ms (5
	End		547.716 ms (5
	Duration		413.872 µs
	Grid Size		[ 64,64,1 ]
	Block Size		[ 32,32,1 ]
	Registers/Thread		10
	Shared Memory/Block		4 KiB
▽	Efficiency		
	Global Load Efficiency		100%
	Global Store Efficiency		100%
	Shared Efficiency	۵	5.9%
	Warp Execution Efficiency		100%
	Non-Predicated Warp Execution Efficien		97.1%
Φ.	Occupancy		
	Achieved		86.7%
	Theoretical		100%
V	Shared Memory Configuration		
	Shared Memory Requested		48 KiB
	Shared Memory Executed		48 KiB

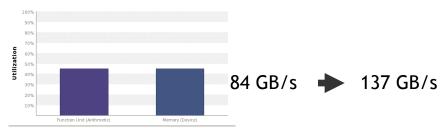
Memory bandwidth is used most efficiently when each shared memory load and store has proper alignment and access pattern.

Optimization: Select each entry below to open the source code to a shared load or store within the kernel with an inefficient alignment or access pattern. For each access pattern of the memory access.

▼ Line / File main.cu - /home/jluitjens/code/CudaHandsOn/Example19 Shared Load Transactions/Access = 16, Ideal Transactions/Access = 1 [ 2097152 transactions for 131072 total executions ]

## Performance Analysis





L1/Shared Memory					
Local Loads	0	0 B/s			
Local Stores	0	0 B/s			
Shared Loads	131072	138.433 GB/s			
Shared Stores	131720	139.118 GB/s			
Global Loads	131072	69.217 GB/s			
Global Stores	131072	69.217 GB/s			
Atomic	0	0 B/s			
L1/Shared Total	524936	415.984 GB/s	Idle	Low	Međiu
L2 Cache					
L1 Reads	524288	69.217 GB/s			
L1 Writes	524288	69.217 GB/s			
Texture Reads	0	0 B/s			
Atomic	0	0 B/s			
Noncoherent Reads	0	0 B/s			
Total	1048576	138.433 GB/s	Idle	Low	* Međiu
Texture Cache					
Reads	0	0 B/s	Idle	Low	Mediu
Device Memory					
Reads	524968	69.306 GB/s			
Writes	524289	69.217 GB/s			

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